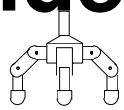
Trident Robotics



and Research, Inc.

TRC004

User's Manual

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Trident Robotics and Research, Inc.
TRC004
PUMA Interface Card

1.0 Introduction

1.1 General Information

The TRC004 is a general purpose interface board for servo applications. It provides eight channels of buffered analog output, eight channels of analog input, six quadrature shaft encoder channels, six bits of discrete input, six bits of discrete output, and a watchdog timer.

The TRC004 is ideally suited for high-performance robotic applications including force-controlled manipulators and dextrous hands. It was specifically designed to replace the LSI/11 VAL computer and servo cards in the Unimate PUMA manipulator to allow high-speed, direct access to joint motor torques and positions.

Its unique design allows it to be placed remotely from the host computer's bus, closer to the noise-sensitive analog plant it is controlling. A generic digital address/data interface links the TRC004 to any one of a wide variety of host bus interface cards that plugs directly into your system. This permits flexibility in upgrading the host computer as technology advances, without incurring the cost of replacing the entire interface card. (Only the inexpensive bus interface must be replaced if a new system bus is chosen.)

The TRC004 is constructed almost entirely of high-speed CMOS integrated circuits that provide rapid access with minimal power drain.

1.2 PUMA-Specific Information

When used as an interface to a Unimate PUMA 550/560 robotic manipulator (and certain 7XX and 2XX series manipulators) with Mark II controller, the TRC004, in conjunction with the user's real-time computer, replaces the entire LSI/11 VAL computer and the joint servo cards. Figure 1.1 shows the VAL controller block diagram as shipped from the factory. Figure 1.2 shows the controller block diagram after removal of the LSI/11 and subsequent installation of the TRC004.

Physically, the CPU, RAM, EPROM, serial controller, interface cards, and joint servos are all removed from the controller backplane. In their place, the TRC004, a single twelve-inch by nine-inch (approximately) multi-purpose I/O card, is mounted and wired point-to-point to the backplane. The TRC004's encoder inputs are connected to the joint encoders of the PUMA for position acquisition. The analog outputs are connected to the power amplifiers for commanding motor torque. The analog inputs are used to measure the potentiometers during calibration. Finally, the discrete inputs and outputs are connected to various housekeeping functions including enabling arm power, controlling the pneumatic hand valves, and monitoring joint thermal sensors.

The burden falls on the user to replace as much of the functionality of the VAL operating system as is desired, including, but not limited to:

- power-on arm calibration
- occasional calibration of the joint potentiometers
- low-level joint position control

Figures 1.1 and 1.2 go here showing the swap in the PUMA

- arm kinematics
- trajectory generation
- joint limit monitoring

The teach pendant, which is a serial peripheral of the LSI/11, becomes non-functional. Any attempt to duplicate its function, both in hardware and software, must be made by the user.

2.0 Specifications

Performance specifications and characteristics of the TRC004 appear in Table 2.1.

3.0 Installation

3.1 General Information

This section of the manual assumes the TRC004 is to be installed in a Unimate PUMA 560 robot with Mark II controller to replace the VAL computer and joint servos. Similar instructions apply to installations in other equipment and for generic lab use so this section should be read and understood by all users. Of course, specific mention to electrical or mechanical connections within the Unimate controller should be extended to analogous components within the user's system. For PUMA robots other than the 560/Mark II, check the appendices for model-specific information.

3.2 VAL Card Removal

Before deactivating the VAL controller, it is suggested that some registration marks be made on the arm to facilitate calibration. To do this, use VAL to put the arm in the ready position by issuing the command "do ready". Turn off arm power and then make two short, narrow marks across each joint from one link to the next. This can be done with a scratch awl or permanent marker. These marks can later be used for positioning the arm by hand to a known configuration for initializing the index pulses of the shaft encoders.

The TRC004 is not designed to plug into the existing card cage of the Unimate controller but, instead, mounts directly on top of it. In order to accomodate this, nearly all of the VAL cards must be removed from the system. Furthermore, the wiring harness for the TRC004 merely parallels the existing wiring, which would result in short circuits if the cards were left in place. (If the user wishes to restore VAL, simply disconnect and remove the TRC004 and replace the VAL cards. The TRC004 wiring need not be removed.)

The cards that must be removed include the entire LSI/11 computer and its peripherals, the interface card and the joint servo cards. The only two cards that remain in the Mark II controller are the Arm Cable Card (slot J58) and the Power Amplifier Control Card (slot J56). Remove all other cards from the Unimate card cage. In the case of a Mark I controller, keep the analog servo cards installed.

3.3 Mounting the TRC004

The TRC004 has nine #6 clearance holes for mounting inside the Unimate controller. At least six of these holes should be used to secure the board to the rails of the Unimate card cage. The recommended orientation is with all holes marked 1 and 2 fastened to the rails of the card cage with nylon screws and half-inch threaded nylon spacers (enclosed). Future revisions of the TRC004 will maintain compatibility with this mounting configuration. It is also desirable to support the overhanging edge of the printed circuit board, thus utilizing all nine of the mounting holes, and to keep the card covered to prevent damage.

The four holes marked "1" form a square whose sides are 5.88 inches center-to-center.

Buffered Analog Outputs	8
D/A Converters	
Input Coding	Negative Offset Binary
Output Range	+/- 10 volts
Resolution	12 bits
Settling time	10 usec max to +/- 1/2 LSB
Linearity Error	+/- 3/4 LSB typical
Op Amp Buffers	
Output Drive	10 mA
Gain	user definable
Accuracy	2% with standard resistors (user definable)
Rolloff Freq.	user definable
Analog Inputs	8
Coding	Positive True Binary
Input Range	0 - 5 volts
Resolution	8 bits
Input Impedance	2500 ohms
Input Capacitance	15 pF
Conversion Time	128 usec
Digital Inputs	6
Signal Type	CMOS/TTL
Digital Outputs	6
Signal Type	TTL Open Collector ("UTIL6" is not open-collector buffered)
Pull-up Resistor	1 K
Sink Current	35 mA
Encoder Inputs	6
Input format	Bi-directional, phase quadrature with index
Signal Type	CMOS/TTL
Counter resolution	16 bits (17 bits for joint 6)
Count Rate	1 MHz max
Operating Temperature	0 - 60 C (performance may degrade near extremes)
Power Requirements	
+5 volts (+0.1/-0.3)	150 mA
+12	50 mA
-12	50 mA

Table 2.1: Specifications of the TRC004

TRIDENT ROBOTICS IS NOT RESPONSIBLE FOR MECHANICAL OR ELECTRICAL DAMAGE TO THE PRINTED CIRCUIT BOARD IN ANY APPLICATION.

3.4 Connections to Unimate Controller

All connections to the Unimate controller are made through connectors P5 and P6 on the TRC004. P6 carries all the logic signals including logic power while P5 carries all the analog signals and analog power. The connections to each mating connector must be made by hand by soldering the appropriate conductors of a ribbon cable to the designated points on the controller backplane. Tables 3.1 and 3.2, plus sheet 2 of the schematics, enumerate the necessary connections between the TRC004 and the Unimate controller while Figure 3.1 shows the layout of the backplane. It is necessary to make all these individual connections because the Unimate backplane is not a true bus architecture. Slots J39 through J58 are all unique, thus no single interface card can tap into all the signals necessary to take control of the sensors and actuators.

Plug P6 mates with jack J6 which must be a 40-pin female header with center-tab polarization. Likewise, plug P5 mates with jack J5 which must be a 34-pin female header with center-tab polarization. Twisted pairs, which are recommended for the DAC lines, can be made from the ribbon cable itself after the J5 header has been attached. To do this, first mark the negative wire of each pair with an indelible pen. Next separate each pair of DAC wires from the adjacent conductors on both sides and simply twist them either by hand or with a low-speed electric drill. Avoid twisting them tighter than a few turns per inch to prevent shorts and broken conductors.

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location
1	POT_J1	J58A-F1	19	DAC+J1	J56A-E1
2	POT_J2	J58A-N1	20	DAC-J1	J56A-E2
3	POT_J3	J58A-V1	21	DAC+J2	J56A-F1
4	POT_J4	J58B-F1	22	DAC-J2	J56A-F2
5	POT_J5	J58B-N1	23	DAC+J3	J56A-H1
6	POT_J6	J58B-V1	24	DAC-J3	J56A-H2
7	POT_J7	J58B-H2	25	DAC+J4	J56A-J1
8	POT_J8	J58A-R2	26	DAC-J4	J56A-J2
9	ADGND	J58A-E2	27	DAC+J5	J56A-K1
10	AD+5V	J58A-F2	28	DAC-J5	J56A-K2
11	NC		29	DAC+J6	J56A-L1
12	NC		30	DAC-J6	J56A-L2
13	+12V	TB1-2F	31	DAC+J7	J55A-E1
14	+12V	TB1-2F	32	DAC-J7	J55A-E2
15	DAGND	TB1-4F	33	DAC+J8	
16	DAGND	TB1-4F	34	DAC-J8	
17	-12V	TB1-3F			
18	-12V	TB1-3F			

Table 3.1: Wiring List for J5 to Unimate Backplane

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location	
1	ENCA1	J58A-A1	21	Vcc	TB1-1F	
2	ENCB1	J58A-C1	22	Vcc	TB1-1F	
3	ENCI1	J58A-E1	23	NC		
4	ENCA2	J58A-H1	24	NC		
5	ENCB2	J58A-K1	25	NC		
6	ENCI2	J58A-M1	26	/STOP	J56A-R2	
7	ENCA3	J58A-P1	27	THERM1	J58A-B1	
8	ENCB3	J58A-S1	28	THERM2	J58A-J1	
9	ENCI3	J58A-U1	29	THERM3	J58A-R1	
10	ENCA4	J58B-A1	30	THERM4	J58B-B1	
11	ENCB4	J58B-C1	31	THERM5	J58B-J1	
12	ENCI4	J58B-E1	32	THERM6	J58B-R1	
13	ENCA5	J58B-H1	33	NC		
14	ENCB5	J58B-K1	34	NC		
15	ENCI5	J58B-M1	35	UTIL1	J56A-T1	/BRAKE
16	ENCA6	J58B-P1	36	UTIL2	J39A-M2	HANDO
17	ENCB6	J58B-S1	37	UTIL3	J39A-L2	HANDC
18	ENCI6	J58B-U1	38	UTIL4		SPARE1
19	GND	TB1-4F	39	UTIL5		SPARE2
20	GND	TB1-4F	40	UTIL6		SPARE3

Table 3.2: Wiring List for J6 to Unimate Backplane

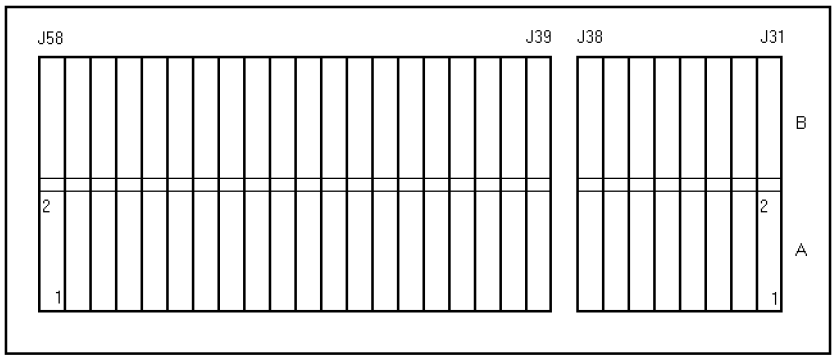

Figure 3.1: Unimate Backplane Layout: Solder Side

3.5 Adjusting Unimate Power Supply

Logic power, Vcc, must be 5V +0.1/- 0.3V. The analog supplies (positive and negative) must be between 12.0V and 14.0V. The TRC004 is equipped with fuses for all three of these power sources. The analog power lines are labeled AD+5V, +12V, and -12V. The logic power line is

labeled Vcc. (AD+5V is the voltage reference for the A/D and is not fused.) It is important that AD+5V does not power up before Vcc or unpredictable A/D operation may result.

The Unimate power supplies run a little high when the cards are removed so it is generally necessary to adjust the voltage levels downward before operating the TRC004. Four of the Unimate's voltage levels are provided by a single power supply and are adjusted by a single potentiometer. To determine if the supplies should be adjusted, use +5V as a reference. If this supply is **below 5.0V,** all supplies will be within the optimal operating range. If not, the supplies must be adjusted.

To do this, first remove AC power and then remove the two power amplifier assemblies. These assemblies are adjacent to the card cage and are secured by four wing nuts. Keep track of all non-metal washers and spacers. The power amplifiers can be removed completely by disconnecting three connectors on each assembly. (Note which connectors go where -- they should be clearly marked.) Beneath the amplifiers is a metal cover which conceals the power supply in question. Lift this cover out of the controller.

Only one potentiometer adjusts all four voltages of this supply. Locate this "pot" near the middle of the board (see figure 3.2). To make the adjustment, AC power must be applied to the controller.

USE EXTREME CAUTION! 120V AC WILL BE PRESENT AND EXPOSED!

Apply power and adjust the pot so the 5V supply is 4.85 - 4.90V. This will provide sufficient margin to accomodate supply variation.

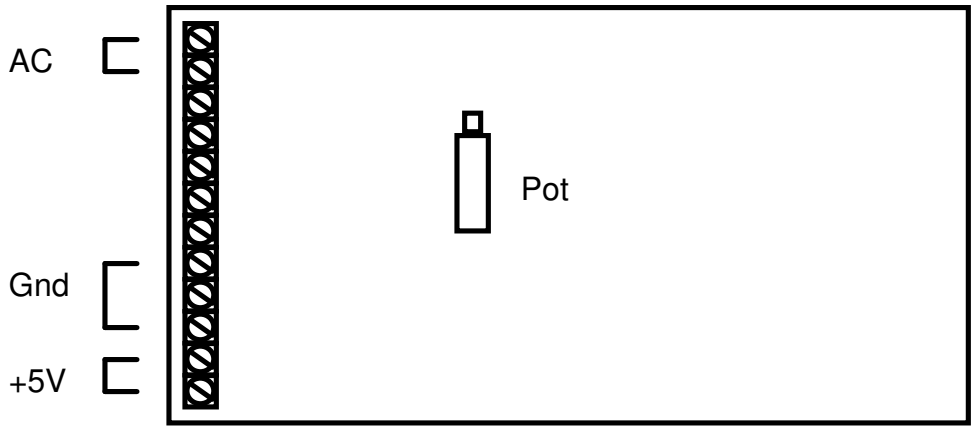

Figure 3.2: Unimate Low-Voltage Power Supply

VERIFY POWER LINES HAVE PROPER VOLTAGE AND POLARITY BEFORE CONNECTING THE TRC004.

DO NOT ATTEMPT TO OPERATE THE CARD WITH ONLY THE LOGIC SUPPLY CONNECTED (+5V). DAMAGE CAN RESULT TO U88, U94 AND U95 IF LOGIC POWER IS APPLIED WITH ANALOG POWER DISCONNECTED.

3.6 Connections to the Bus Interface

A 50-pin ribbon cable, as shown on sheet 3 of the schematics, is used for connections between the TRC004 and the bus interface card (TRC005 or equivalent). The length of this cable should be kept below 3 meters. All 23 ground lines are tied together on the TRC004 and at least one of the ground connections must be made on the bus interface side.

3.7 Index Pulse Phasing

The index pulses of each joint must be adjusted for proper phasing. To accomplish this, a dual-channel oscilloscope must be connected to the 74HC174 integrated circuit of each encoder channel while the corresponding jumper is moved to achieve the desired waveform. The chip and jumper designators for each channel appear in Table 3.3.

ENCODER	74HC174	JUMPER
Channel 1	U1	JP1
Channel 2	U13	JP2
Channel 3	U25	JP3
Channel 4	U37	JP4
Channel 5	U49	JP5
Channel 6	U61	JP6

Table 3.3: Encoder Phasing Components

The two oscilloscope channels must be connected to pins 10 and 13 of the 74HC174 with the oscilloscope synched to pin 13. These pins are marked "TP1" and "TP2" on the circuit board.

NOTE: TO PREVENT THE POSSIBILITY OF SHORTING THE PINS OF THE IC'S, AN IC TEST CLIP (not supplied) SHOULD BE USED TO PERMIT CONNECTION OF THE OSCILLOSCOPE PROBES.

When the joint is moved manually, the index pulses from the encoder appear on pin 13 (TP2). The jumper should be positioned such that pin 10 (TP1) produces one and only one pulse for each pulse appearing on pin 13 and that pulse should be timed such that it is roughly centered with the index pulse (pin 13) as shown in Figure 3.3.

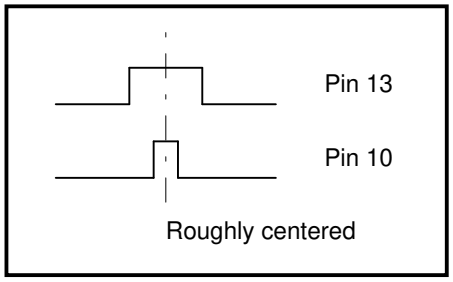

Figure 3.3: Encoder Index Phasing

NOTE: GROUND REFERENCE IS AVAILABLE ON PIN 8 OF THE 74HC174 TO FACILITATE ENCODER PHASING.

4.0 Operations

4.1 General Information

To a host computer, the TRC004 is characterized as a block of 16-bit memory locations as shown in Table 4.1. These locations reside on 16-bit boundaries from the BASE address. THE TRC004 DOES NOT EXAMINE ADDRESS BIT A0 (LSB) FOR ADDRESS DECODING. Therefore, all data transfers must be word size and must be word-aligned. The BASE address is determined by the Bus Interface Card (i.e. TRC005 or equivalent) and is generally user-selectable.

4.2 Analog Outputs

4.2.1 General Information

The TRC004 has eight bipolar, 12-bit analog output channels with op-amp buffers. The digital-to-analog converters (D/A) operate in a fixed +/-10 volt output range. However, the inverting op-amp buffers can be configured by the user to operate at any gain and to provide single-pole filtering if desired.

The output command is encoded as a negative offset binary value. A command value of 0000h results in the maximum positive output voltage, while a command value of 0FFFh results in the maximum negative output voltage. In the default configuration (gain = 1), the maximum positive voltage is +10V and the maximum negative voltage is -10V.

4.2.2 Gain Adjustment

To change the gain of the outputs, the user must physically replace resistor networks RP6 and/or RP7. These are precision resistor networks with eight individual resistors per network. The gain of the inverting op-amp buffer is calculated by:

$$G = -RP6 / RP7$$

and the worst-case gain tolerance is the square root of the sum of the absolute tolerances of the resistor networks. (Resistor network tolerance is typically 2%. Absolute tolerances as high as 0.1% are available.) For greater gain precision, the user can substitute matched resistor networks or resistors of greater absolute accuracy.

NOTE: RESISTANCE VALUES MAY DIFFER FROM THOSE INDICATED ON THE SCHEMATIC.

4.2.3 Filter Adjustment

The single-pole, low-pass filter is configured by adding capacitors to HD8. (See sheet 10 of the TRC004 schematics.) A removable discrete component carrier is provided for this purpose. The cutoff frequency of the filter is calculated by:

$$\omega = 1/(RP6 * HD8) = \text{radians per second}$$
$$f = 1/(2\pi * RP6 * HD8) = \text{hertz.}$$

In the default configuration, no capacitors are included.

4.2.4 Update Procedure

An analog output value is updated by a write to the appropriate address (BASE + 30h + 2*ChannelNumber). The D/A output updates immediately, so no additional update command is necessary.

Register Description	Offset from Base Address	
Joint 1 Index Count	00	
Joint 2 Index Count	02	
Joint 3 Index Count	04	
Joint 4 Index Count	06	
Joint 5 Index Count	08	
Joint 6 Index Count	0A	
Status Input Register	0C	
Unused	0E	**Read Only**
Joint 1 Encoder Count	10	**Locations**
Joint 2 Encoder Count	12	
Joint 3 Encoder Count	14	
Joint 4 Encoder Count	16	
Joint 5 Encoder Count	18	
Joint 6 Encoder Count	1A	
A/D Value	1C	
A/D Start Pulse	1E	
Joint 1 Encoder Load	20	
Joint 2 Encoder Load	22	
Joint 3 Encoder Load	24	
Joint 4 Encoder Load	26	
Joint 5 Encoder Load	28	
Joint 6 Encoder Load	2A	
A/D MUX Channel Select	2C	
Discrete Output Register	2E	**Write Only**
D/A Channel 1 Output	30	**Locations**
D/A Channel 2 Output	32	
D/A Channel 3 Output	34	
D/A Channel 4 Output	36	
D/A Channel 5 Output	38	
D/A Channel 6 Output	3A	
D/A Channel 7 Output	3C	
D/A Channel 8 Output	3E	

Table 4.1: TRC004 Memory Map

4.3 Analog Inputs

4.3.1 General Information

The TRC004 has eight, 8-bit, single-ended analog input channels, multiplexed to a common analog-to-digital converter (A/D). The A/D uses an 8-bit, successive approximation conversion technique. The A/D operates in a fixed 0 - 5 volt input range and the value is encoded in positive binary. An input value of 00h represents a voltage of 0V at the A/D, while a value of FFh represents a voltage of +5V. The most significant 8 bits are undefined and should be stripped off during a read operation.

4.3.2 Update Procedure

An analog input channel is selected by a write to the A/D MUX Channel Select register (BASE + 2Ch). The conversion is then started by a fictitious read to the A/D Start Pulse register (BASE + 1Eh). After 128 milliseconds, when the conversion completes, the A/D value can be read from the A/D Value register (BASE + 1Ch). If the A/D Conversion Mask bit is enabled (logic "1"), the A/D Conversion Status bit is set to "0" to indicate end-of-conversion and the interrupt line goes high.

There are three methods to detect the end-of-conversion:

1.) polling the A/D Conversion Status bit in the Status Input Register
2.) hardware interrupt, if supported by the bus interface card
3.) delay for 128 milliseconds

If polling is used, the A/D Conversion Status bit must be reset to "1" after reading the A/D value. Interrupt operation is generally not recommended for use with the Unimate PUMA because the A/D's are used only at power-up for calibration and are not time-critical.

4.4 Discrete Output Register

4.4.1 General Information

The Discrete Output Register (BASE + 2Eh) is a 16-bit write-only register. (See Figure 4.3.) The lower 5 bits (channels 0 - 4) have inverting, open-collector buffers on their outputs. Bit 5 is a standard CMOS compatible output. These are the only digital outputs for off-board use. The remaining bits provide internal housekeeping, with the exception of bit 15 which controls the red LED, D2.

Upon power-up or system reset, the Discrete Output Register is cleared to 0000h by a hardware timer. This assures that all interrupts and their corresponding status bits are masked. However, the off-board outputs go high when this occurs. In addition, the red LED (D2) turns on.

4.4.2 Calibration Status

Channel 6 is a write-through bit that is normally used to indicate whether or not the encoders have been calibrated. It is set and cleared by the user so its function can be redefined if desired. This bit can be read from the Status Input Register as channel 14. (Note it is shifted 1 byte.)

4.4.3 Bit 17 Preset

Channel 7 is a latched bit used to update the "17th bit" of the channel 5 (joint 6) encoder counter. During an encoder load operation on channel 5, this bit value is stored in both the 0th bit location and the 17th bit location. Which, if either, of these two bits is significant is determined by the user and the setting of jumper JP7. The value of this bit defaults to zero upon power up and reset.

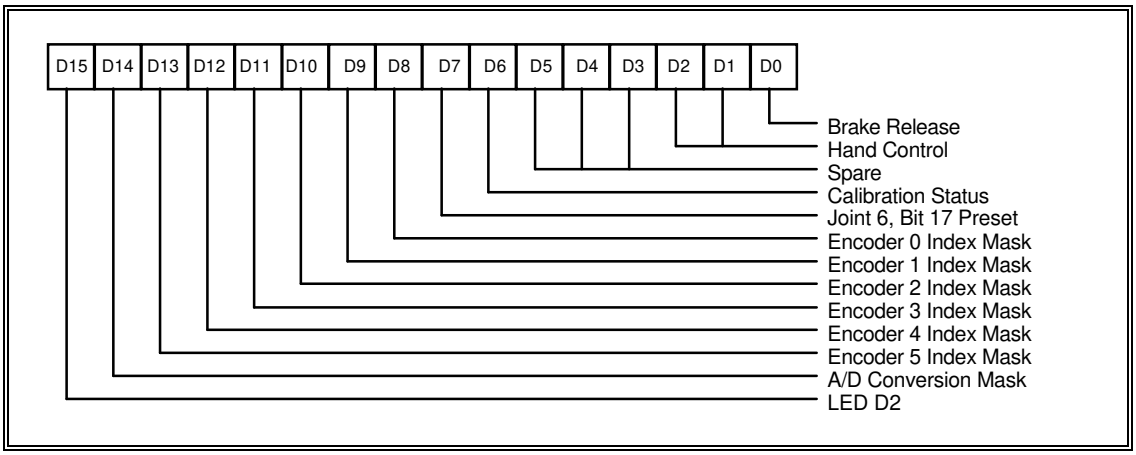

Figure 4.3: Discrete Output Register: Bit fields.

4.4.4 Encoder Index Mask

Channels 8-13 are used to mask/unmask/clear interrupts and bits in the Status Input Register. A logic "0" in the appropriate bit location disables the corresponding interrupt and status bit. A logic "1" enables it. An interrupt is cleared by first disabling it and then re-enabling it.

4.4.5 A/D Conversion Mask

Channel 14 is used to mask/unmask/clear the interrupt and corresponding Status Input Register bit for the A/D Conversion. A logic "0" in the appropriate bit location disables the interrupt and status bit. A logic "1" enables it. An interrupt is cleared by first disabling it and then re-enabling it.

4.4.6 PUMA-Specific Outputs

For use with a PUMA, channel 0 controls the brakes while channels 1 and 2 control the pneumatic hand solenoids. Setting channel 0 low sets the brakes and disables arm power. Setting channel 1 low de-energizes the "hand open" solenoid while setting channel 2 low de-energizes the "hand closed" solenoid. Upon power-up or system reset, these bits are all set low, which sets the brakes and de-energizes both solenoids.

Channels 6 and 7 have been provided specifically for use with the PUMA in a multi-processor, multi-user environment. Channel 6 is intended to be a flag that is updated by software, which indicates whether the arm has been calibrated. "Calibration", in this sense, is the pre-loading of the encoder counters with respect to some world reference frame. Logic "1" means the arm is calibrated. It is reset to zero on power up and system reset.

Channel 7 determines the loading of the "17th bit" of encoder channel 5 and is described in section 4.4.3.

4.4.7 Update Procedure

The Discrete Output Register is written with a 16-bit value to address (BASE + 2Eh). No provisions for bit twiddling are provided and the current value of the register is not readable.

4.5 Status Input Register

4.5.1 General Information

The Status Input Register (BASE + 0Ch) is a 16-bit read-only register. (See Figure 4.4.) Seven bits (channels 0 - 5 and 15) provide the only digital inputs for off-board use. The remaining bits provide interrupt status and internal housekeeping.

4.5.2 Encoder Index Status

Channels 8 - 13 indicate whether or not an index pulse occurred while the corresponding index mask was enabled. A logic "0" represents a pending interrupt, which means an index pulse occurred. These bits can only be cleared by disabling, then re-enabling the mask.

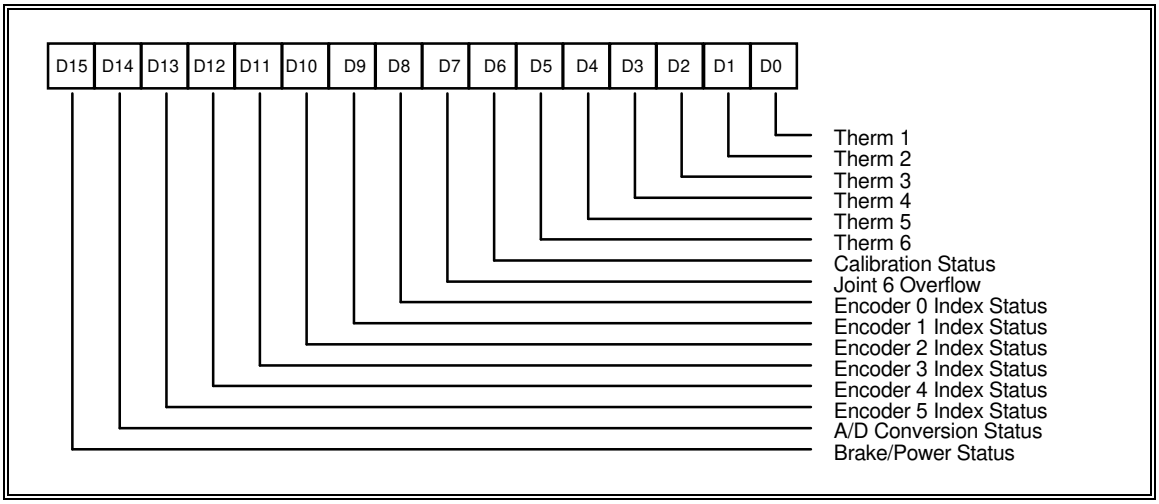

Figure 4.4: Status Input Register: Bit fields.

4.5.3 A/D Conversion Status

Channel 14 indicates whether or not the A/D conversion completed while the mask was enabled. A logic "0" represents a pending interrupt, which means the conversion is complete. This bit can only be cleared by disabling, then re-enabling the mask.

4.5.4 Calibration Status

Channels 6 and 7 have been provided specifically for use with the PUMA in a multi-processor, multi-user environment. Channel 6 is a write-through bit intended to indicate whether the arm has been calibrated. "Calibration", in this sense, is the pre-loading of the encoder counters with respect to some world reference frame. This flag is updated by

software. Logic "1" means the arm is calibrated. It is reset to zero on power up and system reset.

The value of this bit is set by the user through the Discrete Output Register. The meaning of this bit can be re-defined by the user if desired.

4.5.5 Joint 6 Overflow

Channels 6 and 7 have been provided specifically for use with the PUMA in a multi-processor, multi-user environment. Channel 7 reflects the true value of the "17th bit" of the joint 6 encoder counter. It is jumper selectable to indicate bit 0 or bit 17. Encoder channel 6 is logically shifted right one bit so that the 16 bits normally read are bits 1-16, rather than bits 0-15 as is the case for the other encoder counters. This effectively provides a divide-by-two function for joint 6, as required by the PUMA. If dividing by two is not desired, set jumper JP7 to "BIT0" and shift this status bit into the least significant bit in software. If additional range is desired, set jumper JP7 to "BIT17" and append this status bit to bit location 16 in software (sign extending if desired).

Joint six of the PUMA produces more than 65,536 counts per revolution and, in fact, has no mechanical limit stops (allowing infinite rotation). The divide-by-two feature of encoder channel 6 allows the valid 540-degree rotation of joint 6 to fit into a 16-bit word.

4.5.6 PUMA-Specific Inputs

For use with a PUMA, channels 0 - 5 and 15 are dedicated to power and thermal monitoring. Channel 15 indicates the status of arm power. Logic "1" indicates the arm power has been manually energized by the user and the brakes are released. Channels 0 - 5 monitor the thermal switches on the arm itself. Logic "1" indicates thermal overload. (The thermal switches on the power amplifiers directly disable arm power and do not explicitly appear in the Status Input Register.)

Channels 6 and 7 provide a user-definable flag and the value of the "17th bit" for joint 6. These bits are described in sections 4.5.4 and 4.5.5.

4.5.7 Update Procedure

A 16-bit value is read from the Status Input Register at address (BASE + 0Ch). No provisions for bit twiddling are provided.

4.6 Incremental Encoder Inputs

4.6.1 General Information

The TRC004 has six quadrature-phase, incremental encoder counters with 16-bit resolution. The counters are presettable for calibration and an additional latch is provided to store the encoder count at the time an index pulse occurs. Channel 6 automatically divides by two but the 0th bit or the 17th bit is available through the status register to increase the counter's resolution to 17 bits. When connected to a PUMA, the 17th bit is unnecessary.

4.6.2 Encoder Presetting

Each encoder counter can be preset by writing a 16-bit value to the corresponding Encoder Load register (BASE + 20h + 2*ChannelNumber).

Presetting channel 6 requires one additional step. Before loading the encoder counter as described above, the 17th bit (either bit 0 or bit 17) must be set through bit 7 of the Discrete Output Register. This assures the extra bit is loaded simultaneously with the others.

4.6.3 Index Latch

The value of the corresponding encoder counter at the time of its last index pulse can be recovered from the Index Count register (BASE + 00h + 2*ChannelNumber). This latch is updated regardless of the state of the corresponding index mask, but the status bit in the Status Input Register will only go low if the bit is unmasked. The value of channel 6 is divided by two and the 0th or 17th bit cannot be recovered.

4.6.4 Update Procedure

The 16-bit encoder value is read from the corresponding Encoder Count register (BASE + 10h + 2*ChannelNumber).

4.7 Watchdog Timer

4.7.1 General Information

The watchdog timer provides an emergency power-down signal in the event of a controller "crash." The watchdog simply monitors the card for valid write operations and pulses the bit 0 output line if a valid write does not occur every 10-100 milliseconds. The time interval is set at the factory and cannot be changed by the user.

The timeout signal does not latch. It only pulses the output line and automatically resets with the next valid write operation.

4.7.2 Enabling/Disabling

The watchdog timer only operates on bit 0 of the output register which is equivalent to "UTIL1" and "BRK_ON." The watchdog can be disabled by placing jumper JP8 to the right (pins 2 and 3). In this position, no error pulse will be genreated. Placing jumper JP8 to the left (pins 1 and 2) enables the watchdog. The board should not be operated with jumper JP8 removed as the state of bit 0 may be indeterminate.

The green LED (D1) indicates the state of the watchdog timer. The LED turns off when the time interval passes without a valid write operation. However, the LED turns back on immediately after the next write operation so the appearance of a glowing LED may indicate a rapid sequence of error pulses.

4.7.3 Update Procedure

No specific update procedure is required. Any valid write to the TRC004 will reset the watchdog timer and prevent an error signal from being generated for the duration of the time interval. If another valid write is not performed before the expiration of the time interval, an error pulse will be generated at the end of the time interval.

5.0 Troubleshooting

Problem: Index latch never updates
Solution: Index pulse phasing jumper is missing or improperly set. Set encoder index pulse phasing as described in section 3.6.

Problem: Index latch updates continuously
Solution: Index pulse phasing jumper is incorrectly set. Set encoder index pulse phasing as described in section 3.6.

Problem: Index latch count is inconsistent
Solution: Index pulse phasing jumper is incorrectly set. Set encoder index pulse phasing as described in section 3.6.

Problem: Watchdog is enabled and D1 is on but plant power will not turn on
Solution: Update rate may not be fast enough. A glow from the LED is not an indication of timeout-free operation. See section 4.7.

Problem: Inconsistent operation of the A/D converter
Solution: Power-up timing may be incorrect in your application. AD+5V should not power-up before Vcc. See section 3.5 or call Trident Robotics.

Appendix A: Kawasaki PUMA 760/Mark I

Kawasaki was licensed by Unimation to produce PUMA robots. The 760 with Mark I controller was one of the robots produced under this licensing agreement.

The Mark I controller has separate analog and digital servo boards. In order to operate in conjunction with the TRC004, the analog servo cards (slots J49 - J54) and the clock card (slot J48) must remain in the card cage. The digital servo cards are removed along with the other cards specified in section 3.2. As always, the cable card, J58, remains.

Connections to J5 and J6 are somewhat different as a result of the analog servo cards. The correct backplane connections are shown in tables A.1 and A.2, respectively. The THERM lines can be used as user input lines or tied high as shown. It is also necessary to tie AE1, AP2, and AR1 of the analog servo cards for joints 4-6 (slots J52 - J54) low.

The ENCI lines are treated differently, also. A separate 4.7K resistor should connect each of these lines to ground. The affected backplane positions are J58A-E1, J58A-M1, J58A-U1, J58B-E1, J58B-M1, and J58B-U1. Use proper care to prevent short circuits.

As a final note, the user must ensure AD+5V does not power up before Vcc. Check your system with an oscilloscope. If AD+5V exceeds Vcc by more than 0.1V at any time, unpredictable A/D operation can result. If this is the case, one of two approaches can be used to eliminate the problem. The first method is to put a 100 ohm resistor in the AD+5V line and connect it to Vcc on the Kawasaki backplane. Then place a capacitor of a few microfarads from the resistor to ground. (Do not connect the capacitor to the side of the resistor that is connected to Vcc.) Alternatively, a separate +5V voltage regulator can be added to produce Vcc from the +12V source using appropriate filter capacitors. These modifications are shown in Figure A.1.

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location
1	POT_J1	J58A-F1	19	DAC+J1	J49A-S2
2	POT_J2	J58A-N1	20	DAC-J1	J49A-U2
3	POT_J3	J58A-V1	21	DAC+J2	J50A-S2
4	POT_J4	J58B-F1	22	DAC-J2	J50A-U2
5	POT_J5	J58B-N1	23	DAC+J3	J51A-S2
6	POT_J6	J58B-V1	24	DAC-J3	J51A-U2
7	POT_J7	J58B-H2	25	DAC+J4	J52A-S2
8	POT_J8	J58A-R2	26	DAC-J4	J52A-U2
9	ADGND	J58A-E2	27	DAC+J5	J53A-S2
10	AD+5V	J58A-F2	28	DAC-J5	J53A-U2
11	NC		29	DAC+J6	J54A-S2
12	NC		30	DAC-J6	J54A-U2
13	+12V	TB1-2F	31	DAC+J7	J55A-S2
14	+12V	TB1-2F	32	DAC-J7	J55A-U2
15	DAGND	TB1-4F	33	DAC+J8	
16	DAGND	TB1-4F	34	DAC-J8	
17	-12V	TB1-3F			
18	-12V	TB1-3F			

Table A.1: Wiring List for J5 to Kawasaki Backplane

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location	
1	ENCA1	J49B-E2	21	Vcc	TB1-1F	
2	ENCB1	J49B-H2	22	Vcc	TB1-1F	
3	ENCI1	J58A-E1	23	NC		
4	ENCA2	J50B-E2	24	NC		
5	ENCB2	J50B-H2	25	NC		
6	ENCI2	J58A-M1	26	/STOP	J48B-A1	
7	ENCA3	J51B-E2	27	THERM1	Vcc	
8	ENCB3	J51B-H2	28	THERM2	Vcc	
9	ENCI3	J58A-U1	29	THERM3	Vcc	
10	ENCA4	J52B-E2	30	THERM4	Vcc	
11	ENCB4	J52B-H2	31	THERM5	Vcc	
12	ENCI4	J58B-E1	32	THERM6	Vcc	
13	ENCA5	J53B-E2	33	NC		
14	ENCB5	J53B-H2	34	NC		
15	ENCI5	J58B-M1	35	UTIL1	J48B-H1	/BRAKE
16	ENCA6	J54B-E2	36	UTIL2	J58A-T2	HANDO
17	ENCB6	J54B-H2	37	UTIL3	J58A-S2	HANDC
18	ENCI6	J58B-U1	38	UTIL4		SPARE1
19	GND	TB1-4F	39	UTIL5		SPARE2
20	GND	TB1-4F	40	UTIL6		SPARE3

Table A.2: Wiring List for J6 to Kawasaki Backplane

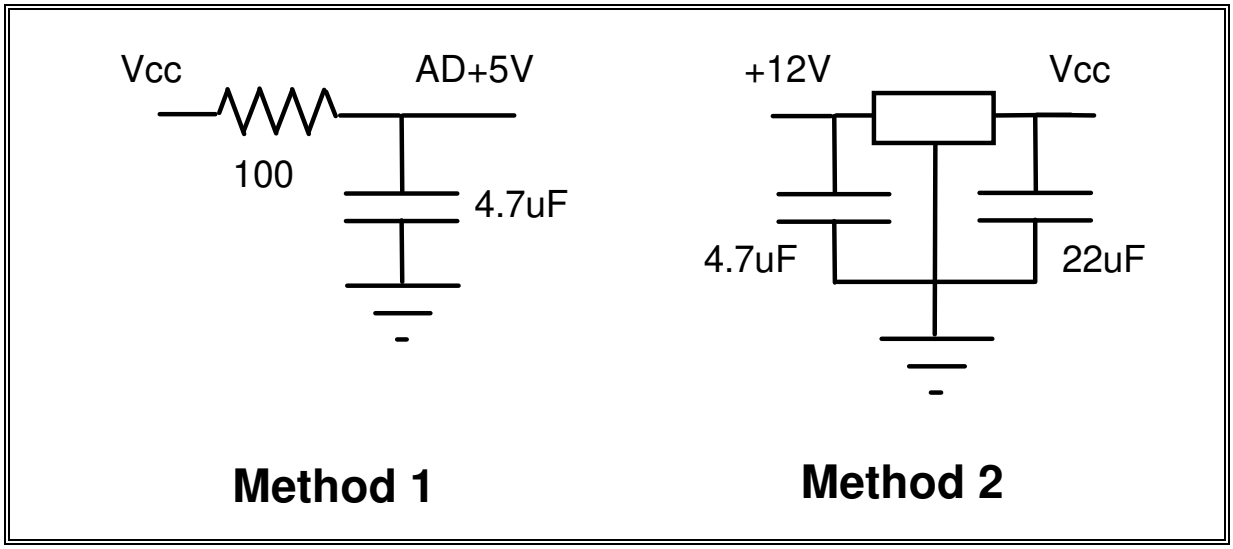

Figure A.1: Suggested methods to correct power-up timing.

Jumpers JP9, JP10, and JP11 on the TRC004 card remain in the normal (NOR) position.

Appendix B: Unimate PUMA 560 with 26-slot Backplane

Some later versions of the Unimate backplane have 26 slots (J31 - J56) and signals are routed entirely on the printed circuit board as opposed to partial wire wrap. There is also no physical division between the CPU cards and the servo cards (although the differences in backplane bussing remain). This backplane configuration appears in figure B.1.

Slots J31 - J43 are reserved for LSI/11 support cards. These support cards include the A Interface Card which resides in slot J43. The B Interface Card resides in slot J44 which marks the beginning of the low-level control backplane. This secondary backplane extends from slot J44 - J56. The Digital Servo Cards occupy slots J45 - J50. The Power Amplifier Control Card and Arm Cable Card occupy slots J55 and J56, respectively.

As described in section 3.2, remove all cards except the Power Amplifier Control Card (slot J55) and the Arm Cable Card (slot J56). The modified backplane wiring lists appear in tables B.1 and B.2.

Jumpers JP9, JP10, and JP11 on the TRC004 card remain in the normal (NOR) position.

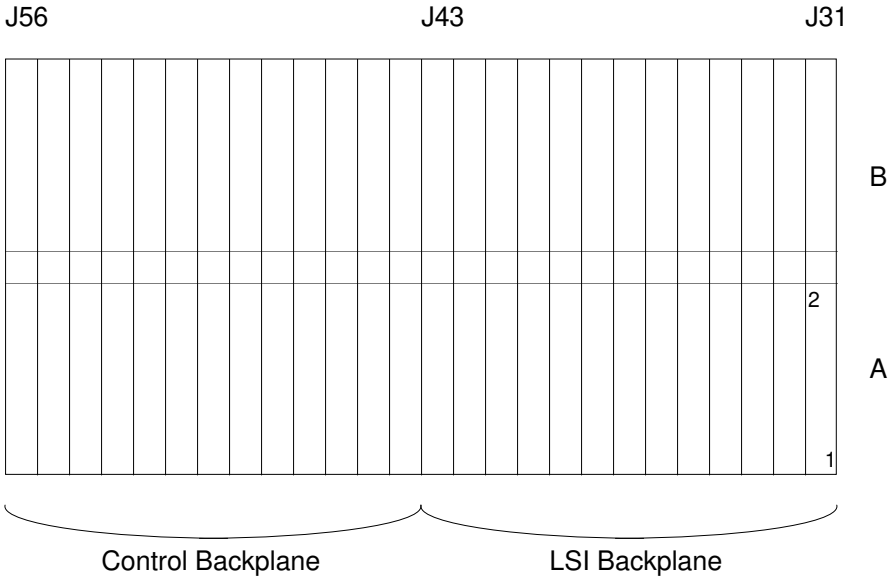

Figure B.1: Unimate Backplane Layout: Solder Side

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location
1	POT_J1	J56A-F1	18	-12V	TB1-3F
2	POT_J2	J56A-N1	19	DAC+J1	J55A-E1
3	POT_J3	J56A-V1	20	DAC-J1	J55A-E2
4	POT_J4	J56B-F1	21	DAC+J2	J55A-F1
5	POT_J5	J56B-N1	22	DAC-J2	J55A-F2
6	POT_J6	J56B-V1	23	DAC+J3	J55A-H1
7	POT_J7	J56B-H2	24	DAC-J3	J55A-H2
8	POT_J8	J56A-R2	25	DAC+J4	J55A-J1
9	ADGND	J56A-E2	26	DAC-J4	J55A-J2
10	AD+5V	J56A-F2	27	DAC+J5	J55A-K1
11	NC		28	DAC-J5	J55A-K2
12	NC		29	DAC+J6	J55A-L1
13	+12V	TB1-2F	30	DAC-J6	J55A-L2
14	+12V	TB1-2F	31	DAC+J7	
15	DAGND	TB1-4F	32	DAC-J7	
16	DAGND	TB1-4F	33	DAC+J8	
17	-12V	TB1-3F	34	DAC-J8	

Table B.1: Wiring List for J5 to Unimate Backplane

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location	
1	ENCA1	J56A-A1	21	Vcc	TB1-1F	
2	ENCB1	J56A-C1	22	Vcc	TB1-1F	
3	ENCI1	J56A-E1	23	NC		
4	ENCA2	J56A-H1	24	NC		
5	ENCB2	J56A-K1	25	NC		
6	ENCI2	J56A-M1	26	/STOP	J55A-R2	
7	ENCA3	J56A-P1	27	THERM1	J56A-B1	
8	ENCB3	J56A-S1	28	THERM2	J56A-J1	
9	ENCI3	J56A-U1	29	THERM3	J56A-R1	
10	ENCA4	J56B-A1	30	THERM4	J56B-B1	
11	ENCB4	J56B-C1	31	THERM5	J56B-J1	
12	ENCI4	J56B-E1	32	THERM6	J56B-R1	
13	ENCA5	J56B-H1	33	NC		
14	ENCB5	J56B-K1	34	NC		
15	ENCI5	J56B-M1	35	UTIL1	J55A-T1	/BRAKE
16	ENCA6	J56B-P1	36	UTIL2	J44A-M2	HANDO
17	ENCB6	J56B-S1	37	UTIL3	J44A-L2	HANDC
18	ENCI6	J56B-U1	38	UTIL4		SPARE1
19	GND	TB1-4F	39	UTIL5		SPARE2
20	GND	TB1-4F	40	UTIL6		SPARE3

Table B.2: Wiring List for J6 to Unimate Backplane

Appendix C: Unimate PUMA 760 with Mark III Controller

The Mark III controller is electrically similar to the Mark II controller. The primary differences are in the mechanical layout of the components. The power amplifiers are the most obviously different components (all amplifiers are physically separate with joints 1-3 having considerably greater current capability) and there are two separate card cages for *signal* components and *power* components.

With the exception of the /STOP signal, the signal components card cage contains all the signals of interest for the installation of the TRC004 and this card cage is similar in layout to the card cage in Appendix B. (Slot J55 is electrically different, however.) The backplane configuration of this card cage appears in figure C.1.

Slots J31 - J43 are reserved for LSI/11 support cards. These support cards include the A Interface Card which resides in slot J43. The B Interface Card resides in slot J44 which marks the beginning of the low-level control backplane. This secondary backplane extends from slot J44 - J56. The Digital Servo Cards occupy slots J45 - J50. Slot J55, formerly dedicated to the Power

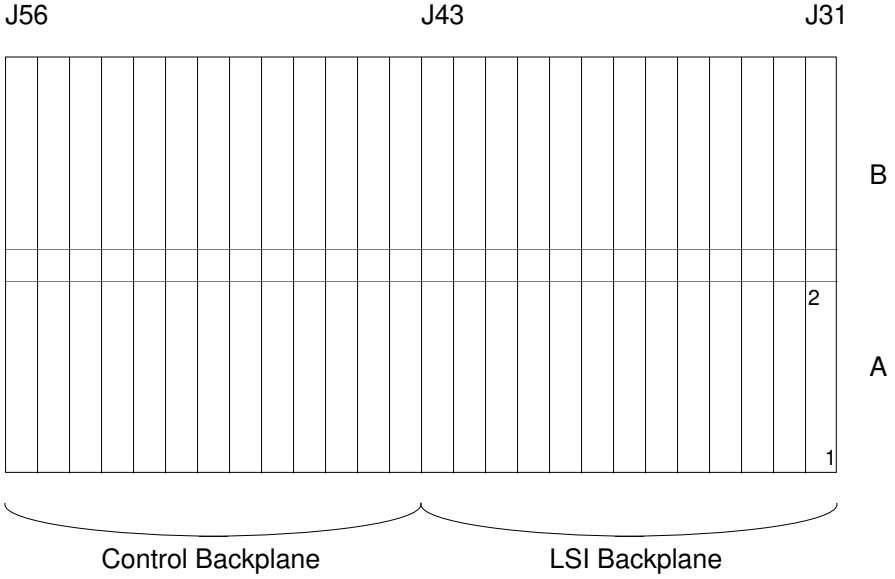

Figure C.1: Unimate Backplane Layout: Solder Side

Amplifier Control Card, is vacant in the Mark III while the Arm Cable Card occupies slot J56, as in the 26-slot Mark II.

As described in section 3.2, remove all cards except the Arm Cable Card (slot J56). The modified backplane wiring lists appear in tables B.1 and B.2.

Jumpers JP9, JP10, and JP11 on the TRC004 card remain in the normal (NOR) position.

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location
1	POT_J1	J56A-F1	18	-12V	TB5-4
2	POT_J2	J56A-N1	19	DAC+J1	J103-11
3	POT_J3	J56A-V1	20	DAC-J1	J103-12
4	POT_J4	J56B-F1	21	DAC+J2	J103-13
5	POT_J5	J56B-N1	22	DAC-J2	J103-14
6	POT_J6	J56B-V1	23	DAC+J3	J103-15
7	POT_J7	J56B-H2	24	DAC-J3	J103-16
8	POT_J8	J56A-R2	25	DAC+J4	J103-17
9	ADGND	J56A-E2	26	DAC-J4	J103-18
10	AD+5V	J56A-F2	27	DAC+J5	J103-19
11	NC		28	DAC-J5	J103-20
12	NC		29	DAC+J6	J103-21
13	+12V	TB5-3	30	DAC-J6	J103-22
14	+12V	TB5-3	31	DAC+J7	J103-23
15	DAGND	TB5-2	32	DAC-J7	J103-24
16	DAGND	TB5-2	33	DAC+J8	J103-25
17	-12V	TB5-4	34	DAC-J8	J103-26

Table C.1: Wiring List for J5 to Unimate Backplane

Pin #	Signal Name	Backplane Location	Pin #	Signal Name	Backplane Location	
1	ENCA1	J56A-A1	21	Vcc	TB5-1	
2	ENCB1	J56A-C1	22	Vcc	TB5-1	
3	ENCI1	J56A-E1	23	NC		
4	ENCA2	J56A-H1	24	NC		
5	ENCB2	J56A-K1	25	NC		
6	ENCI2	J56A-M1	26	/STOP	J69-12c	
7	ENCA3	J56A-P1	27	THERM1	J56A-B1	
8	ENCB3	J56A-S1	28	THERM2	J56A-J1	
9	ENCI3	J56A-U1	29	THERM3	J56A-R1	
10	ENCA4	J56B-A1	30	THERM4	J56B-B1	
11	ENCB4	J56B-C1	31	THERM5	J56B-J1	
12	ENCI4	J56B-E1	32	THERM6	J56B-R1	
13	ENCA5	J56B-H1	33	NC		
14	ENCB5	J56B-K1	34	NC		
15	ENCI5	J56B-M1	35	UTIL1	J103-5	/BRAKE
16	ENCA6	J56B-P1	36	UTIL2	J44A-M2	HANDO
17	ENCB6	J56B-S1	37	UTIL3	J44A-L2	HANDC
18	ENCI6	J56B-U1	38	UTIL4		SPARE1
19	GND	TB5-2	39	UTIL5		SPARE2
20	GND	TB5-2	40	UTIL6		SPARE3

Table C.2: Wiring List for J6 to Unimate Backplane

Appendix D: Schematics

Complete schematics of the TRC004 follow.